IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of

FLYNN et al — Atty. Ref.: 550-466

Serial No. 10/691,501 — Group: 2189

Filed: October 23, 2003 — Examiner: Dinh, Ngoc V.

For: HARDWARE DRIVEN STATE SAVE/RESTORE IN A DATA PROCESSING SYSTEM

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April 6, 2009

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

I. REAL PARTY IN INTEREST

- The real party in interest is the assignee, ARM Limited, a United Kingdom corporation.

II. RELATED APPEALS AND INTERFERENCES

- There are no other appeals related to this subject application.

There are no interferences related to this subject application.

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BRIEF FOR APPELLANT

On Appeal From Final Rejection
From Group Art Unit 2189

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III. STATUS OF CLAIMS

- Claims 1-24 are pending, rejected, and on appeal.

IV. STATUS OF AMENDMENTS

- No amendments after final were filed.[1]

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

A data processing system should be able to save and restore its system state. One situation where this is helpful is in a power saving or power-down mode. For example, if the system detects it has been idle for a predetermined amount of time or that a power down key was pressed, the system can switch to a power-down mode. But when the power-down mode is exited, the system should return to its previous state unaltered so that processing operations can continue smoothly and efficiently. Otherwise, if the information/state is lost upon exiting the power-down mode, a full system reboot and initialization upon restart must be performed.

One approach to power-saving power-down uses a power-down software routine executed when entry to the power-down mode is required. The routine saves to some non-volatile storage data that captures the state of the system. A

[1] A pre-appeal was filed on June 18, 2007 followed by a first appeal brief. The Examiner applied a new primary reference in each of the two office actions issued after the first appeal brief.

complementary piece of software can be run when the system resumes operation to restore this state information from the non-volatile storage so that processing can be recommenced at the same point and with the same system state. But a significant disadvantage with this approach is slow software routine execution when storing the system state and then to later when restoring the system state. Furthermore, there may be some system state information which is not accessible to the software responsible for saving the system state, such as for example cache memory contents, tightly-coupled memory contents, and other, relatively low level hardware state information. In such circumstances, when processing is resumed, it recommences in a way that only approximates the state of the system when power-down occurred, such as for example there being a requirement to refill all of the cache memories, which may be a relatively slow and power consuming operation. Furthermore, upon restarting the system, some state information required for a restart, such as a page table mapping, is not available.

The inventors found a better way to save data values representing the system state using the existing system bus and memory within a data processing system under the control of a state saving controller. Surprisingly, by reusing the already-provided system bus and memory, the state saving controller can be simple and yet rapidly and efficiently save and later restore the system state with an advantageous degree of completeness.

The following is a mapping of independent claim 1 onto an example, non-limiting embodiment in the specification.[2]

Apparatus for processing data, comprising:	Figure 2.
a circuit used in processing data, said circuit having one or more nodes for storing one or more data values that together define a state of said circuit;	Processor core 2 stores one or more data values in one or more nodes like registers, program counters, etc. coupled to scan chains 12. See Figure 3 and page 8, lines 4-6 and 12-14.
a memory for storing data;	Memory 14 in Figure 3. See page 8, lines 4-6.
a multi-bit wide system bus, coupled to said circuit and said memory, for transferring multi-bit data words between said circuit and said memory in response to memory transfer requests issued upon said system bus during normal processing operation of said circuit and said memory; and	A multi-bit wide system bus 6 , 8, and 10 couples core 2 and memory 14 and transfers multi-bit data words between the circuit and memory in response to memory transfer requests issued upon the bus 6 during normal processing operation. Page 8, lines 15-17.
a state saving controller, coupled to said circuit and said system bus, configured in response to a state saving trigger to read said data values defining a state of said circuit from said one or more nodes and to	State saving controller 16 responds to a state saving trigger to read said data values defining a state of said circuit from one or more nodes coupled to a scan chain 12. The

[2] This mapping in no way limits the claim scope and is not intended to be used in construing the meaning of claim terms. Indeed, another non-limiting example embodiment is described in conjunction with Figure 5.

generate a sequence of memory write requests on said system bus that write one or more state saving multi-bit data words representing said data values into said memory such that said state of said circuit is restorable using said one or more state saving multi-bit data words.	controller 16 then clocks the scan chains 12 to form the state saving data words and generate the address control signal on the bus to cause a data transfer from the core 2 to memory 14. A restore operation is described at page 8, lines 27-32.

Because independent method claim 13 is a method analog of apparatus claim 1, the mapping provided for claim 1 also applies to independent claim 13.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

- The first rejection on appeal is the rejection of claims 1-7, 9, 11-19, 21, 23, and 24 under 35 U.S.C. §103 as being unpatentable over Woods (7,058,834) in view of Langford (5,115,435).
- The second rejection on appeal is the rejection of claims 8 and 20 under 35 U.S.C. §103 as being unpatentable over Woods (7,058,834) in view of Langford (5,115,435) and further in view of Perner (6,728,799).
- The third rejection on appeal is the rejection of claims 10 and 22 under 35 U.S.C. §103 as being unpatentable over Woods (7,058,834) in view of Langford (5,115,435) and further in view of Borden (5,790,561).

VII. ARGUMENT

The Rejection Of Claims 1-7, 9, 11-19, 21, 23, And 24 Under 35 U.S.C. §103 As Being Unpatentable Over Woods And Langford Is Improper

A. The Legal Requirements For Obviousness

An invention is obvious only "if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains." 35 U.S.C. §103. Obviousness is a legal conclusion based on underlying findings of fact. *In re Dembiczak,* 175 F.3d 994, 998 (Fed. Cir. 1999). The underlying factual inquiries are: "(1) the scope and content of the prior art; (2) the level of ordinary skill in the prior art; (3) the differences between the claimed invention and the prior art; and (4) objective evidence of nonobviousness." *Id.*

In *KSR International Co. v. Teleflex, Inc.,* 127 S. Ct. 1727, 1739 (2007), the Supreme Court rejected the Federal Circuit's rigid application of the teaching-suggestion-motivation ("TSM") test. However, in evaluating obviousness in light of multiple patents, a determination must still be made "whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *Id.* at 1741. "[T]his analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the

art would employ." *Id.* Nevertheless, the Examiner must still provide an explicit analysis with supported, articulated reasoning, that includes "an apparent reason to combine the known elements" in the manner claimed. *See Id.* at 1740-41 ("To facilitate review, this analysis should be made explicit."). The Supreme Court stated that this requirement cannot be satisfied by conclusory statements without articulated reasoning and some rational underpinning to support the legal conclusion of obviousness. *Id.* at 1741.

B. Woods

Woods discloses an integrated circuit 130 in which state data is saved in a memory 270 that forms part of an interactive state power reduction manager (ISPRM) 160 as illustrated in Figure 2. The state data is serially scanned in and out of the memory 270 via the serial signal paths 234 and 232. The memory 270 used for state saving and state restoring is part of the ISPRM 160 and is not disclosed as the memory used during normal processing operation of the integrated circuit 130.

C. Langford

Langford discloses a system for increasing the speed of boundary scan test operations of an integrated circuit 10 by using existing address and data buses 14, 16 to transfer test data into the integrated circuit 10 for boundary scan and test results out of the integrated circuit following boundary scan. During the boundary scan test mode, the data inputs and data outputs of the integrated circuit are

switched from the normal input and output connections, and a test word is input via the buses or a test response output via the buses using an external system data bus. See column 3, lines 9-17. This data transfer during testing is with an external testing circuit and not with the memory used during normal operation of the integrated circuit. This external system is the test processor referred to at the end of the Abstract.

D. The Combination of Woods and Langford Fails to Teach Using the Same Memory Used in Normal Operation to Also Store State Data in Response to a State Saving Trigger

The final office action maps the claimed memory onto the special memory 270 in Woods. See the bottom of page 3 of the final action. The independent claims specify that the multi-bit wide system bus transfers "multi-bit data words between said circuit and said memory ... during normal processing operation of said circuit and said memory." This is not the case with Woods in which the memory 270 is a special purpose memory (see column 7, lines 21-32) provided for the purpose of save and restore and is not the memory used during normal processing operation. This feature of the independent claims, i.e., use of the same system bus and the same memory for both the normal processing operations and to also store the state data in response to a state saving trigger with the state data being written to that memory via the system bus is not taught in Woods.

Column 3, lines 12 to 35 of Woods describes two modes of operation: a state saving mode and a normal mode. Woods uses the term "normal" to refer to

the non-state saving operation of the system. In the normal mode of operation in Woods, the memory 270 is not used. Instead, memory 270 is dedicated to state saving mode.

The Examiner argues that making something integral or separable is not patentable. But this misses the point. The independent claims do not recite making the state saving memory integral to or separate from the rest of the apparatus. Rather, these claims describe reusing the same memory and system bus used during normal processing operations to also provide the storage of state data in response to a state saving trigger.

The Examiner acknowledges that Woods also does not teach the claimed multi-bit wide system bus and seeks to draw this teaching from Langford. Langford discloses multi-bit address and data buses 14, 16 used during boundary scan testing to communicate with an external test processor and not with a memory that is used during normal operation. Indeed, Langford states at col. 4, lines 36-42:

> During normal operation, these buses 14, 16 communicate address and data information between IC logic functions 18 and a larger external system (not shown). However, during a test operation, the buses 14, and 16 communicate with the boundary scan test circuit 12 primarily, and with the IC logic functions 18 as required by the test operation.

This text makes it is clear that during test operation, the buses 14 and 16 do not store the state information in a normal operation memory.

Thus, even if the combination of Woods and Langford were made, for purposes of argument only, this combination would not result in a teaching of (1) a multi-bit wide system bus transferring "multi-bit data words between said circuit and said memory in response to memory transfer requests issued upon said system bus during normal processing operation of said circuit and said memory" and (2) writing "one or more state saving multi-bit data words representing said data values [defining a state of the circuit] into said memory such that said state of said circuit is restorable using said one or more state saving multi-bit data words."

The Rejection Of Claims 8 and 20 Under 35 U.S.C. §103 As Being Unpatentable Over Woods, Langford, And Perner Is Improper

Perner fails to remedy the deficiencies noted above with respect to Woods and Langford concerning the independent claims. Therefore, the rejection of claims 8 and 20 is improper for at least the reasons set forth above.

The Rejection Of Claims 10 and 22 Under 35 U.S.C. §103 As Being Unpatentable Over Woods, Langford, and Borden Is Improper

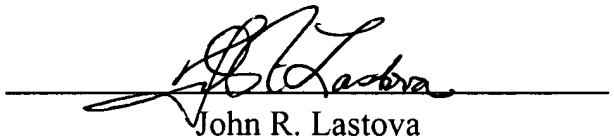
Borden fails to remedy the deficiencies noted above with respect to Woods and Langford concerning the independent claims. Therefore, the rejection of claims 10 and 22 is improper for at least the reasons set forth above.

VIII. CONCLUSION

The obviousness rejections are in error because the combination of Woods and Langford lacks features from the independent claims. The Board should reverse the rejection and order the application allowed.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 

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Appendix A - Claims on Appeal

IX. CLAIMS APPENDIX

1. (Previously presented) Apparatus for processing data, comprising:

a circuit used in processing data, said circuit having one or more nodes for storing one or more data values that together define a state of said circuit;

a memory for storing data;

a multi-bit wide system bus, coupled to said circuit and said memory, for transferring multi-bit data words between said circuit and said memory in response to memory transfer requests issued upon said system bus during normal processing operation of said circuit and said memory; and

a state saving controller, coupled to said circuit and said system bus, configured in response to a state saving trigger to read said data values defining a state of said circuit from said one or more nodes and to generate a sequence of memory write requests on said system bus that write one or more state saving multi-bit data words representing said data values into said memory such that said state of said circuit is restorable using said one or more state saving multi-bit data words.

2. (Original) Apparatus as claimed in claim 1, wherein said circuit is a processor core.

3. (Original) Apparatus as claimed in claim 1, wherein said one or more nodes are each coupled to a respective scan chain cell within said circuit, said state saving controller being operable in response to said state saving trigger to store said data values within respective scan chain cells and to serially read said data values from said scan chain cells to form said one or more state saving multi-bit data words.

4. (Original) Apparatus as claimed in claim 3, comprising a plurality of scan chains each containing a plurality of scan chain cells, said plurality of scan chains operating in parallel to provide respective bits that together form a state saving multi-bit data word as said plurality of scan chains of serially read.

5. (Original) Apparatus as claimed in claim 3, wherein said scan chain cells are also operable to perform test functions upon said circuit.

6. (Original) Apparatus as claimed in claim 1, wherein said circuit is a further memory and said data values are bits of data words stored in said further memory.

7. (Original) Apparatus as claimed in claim 6, wherein said further memory is coupled to a built-in self-test controller operable to perform self-test operations upon said further memory and said state saving controller uses said built-in self-test controller to read data values from said further memory to form said state saving multi-bit data words.

8. (Original) Apparatus as claimed in claim 1, wherein said memory transfers are burst mode memory transfers.

9. (Original) Apparatus as claimed in claim 1, wherein said state saving controller is operable in response to a state restoring trigger to generate a sequence of memory read requests on said system bus that read said one or more multi-bit state saving data words from said memory via said system bus and write said data values represented by said multi-bit state saving data words to said one or more nodes to thereby restore said state of said circuit.

10. (Original) Apparatus as claimed in claim 1, wherein said multi-bit state saving data words are stored in a user specified region of said memory.

11. (Original) Apparatus as claimed in claim 1, wherein said state saving trigger comprises execution of a state saving program instruction.

12. (Original) Apparatus as claimed in claim 1, wherein said state saving trigger comprises initiation of a diagnostic test upon said circuit.

13. (Original) A method of saving state within an apparatus for data processing having:

a circuit used in processing data, said circuit having one or more nodes operable to store one or more data values that together define a state of said circuit;

a memory operable to store data; and

a system bus coupled to said circuit and said memory and operable to transfer multi-bit data words between said circuit and said memory in response to memory transfer requests issued upon said system bus during normal processing operation of said circuit and said memory; said method comprising:

in response to a state saving trigger, using a state saving controller coupled to said circuit and said system bus to read said data values defining a state of said circuit from said one or more nodes and to generate a sequence of memory write requests on said system bus that write one or more state saving multi-bit data words representing said data values into said memory such that said state of said circuit is restorable using said one or more state saving multi-bit data words.

14. (Original) A method as claimed in claim 13, wherein said circuit is a processor core.

15. (Original) A method as claimed in claim 13, wherein said one or more nodes are each coupled to a respective scan chain cell within said circuit, said state saving

controller being operable in response to said state saving trigger to store said data values within respective scan chain cells and to serially read said data values from said scan chain cells to form said one or more state saving multi-bit data words.

16. (Original) A method as claimed in claim 15, comprising a plurality of scan chains each containing a plurality of scan chain cells, said plurality of scan chains operating in parallel to provide respective bits that together form a state saving multi-bit data word as said plurality of scan chains of serially read.

17. (Original) A method as claimed in claim 15, wherein said scan chain cells are also operable to perform test functions upon said circuit.

18. (Original) A method as claimed in claim 13, wherein said circuit is a further memory and said data values are bits of data words stored in said further memory.

19. (Original) A method as claimed in claim 18, wherein said further memory is coupled to a built-in self-test controller operable to perform self-test operations upon said further memory and said state saving controller uses said built-in self-test controller to read data values from said further memory to form said state saving multi-bit data words.

20. (Original) A method as claimed in claim 13, wherein said memory transfers are burst mode memory transfers.

21. (Original) A method as claimed in claim 13, wherein said state saving controller is operable in response to a state restoring trigger to generate a sequence of memory read requests on said system bus that read said one or more multi-bit state saving data words from said memory via said system bus and write said data values represented by said multi-bit state saving data words to said one or more nodes to thereby restore said state of said circuit.

22. (Original) A method as claimed in claim 13, wherein said multi-bit state saving data words are stored in a user specified region of said memory.

23. (Original) A method as claimed in claim 13, wherein said state saving trigger comprises execution of a state saving program instruction.

24. (Original) A method as claimed in claim 13, wherein said state saving trigger comprises initiation of a diagnostic test upon said circuit.

X. EVIDENCE APPENDIX

There is no evidence appendix.

XI. RELATED PROCEEDINGS APPENDIX

There is no related proceedings appendix.